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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,451	08/27/2003	Subhas C. Bose Jayappa Veeramma	011775-013210US	7137

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TOWNSEND AND TOWNSEND AND CREW, LLP
TWO EMBARCADERO CENTER
EIGHTH FLOOR
SAN FRANCISCO, CA 94111-3834

EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

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03/03/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/650,451	BOSE JAYAPPA VEERAMMA ET AL.	
	Examiner	Art Unit	
	Ori Nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 December 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 26-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 26-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

In view of the appeal brief filed on 10/07/2009, PROSECUTION IS HEREBY REOPENED. A new ground of rejection is set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing below:

/Lynne A. Gurley/

Supervisory Patent Examiner, Art Unit 2811

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 25-26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano (5,138,415) in view of Gross (5,316,964) and Patterson (4,972,247).

Yano teaches in figure 2 and related text a power device, comprising:

a semiconductor substrate 16 of first conductivity having an upper surface and a lower surface;

a first electrode terminal 29 coupled to a first conductive region 24 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal 36 coupled to a second conductive region 18 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region 17 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

a passivation layer 28 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Yano does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least

partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, in Yano's device in order to provide better protection to the device and to increase the electrical isolation capabilities of the device.
The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41).
Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 26, prior art's device includes a passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

Regarding claim 28, the claimed limitations of "the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region" are inherent in prior art's device, because prior art's device comprises a peripheral junction region which compensates the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region, as claimed.

Regarding claim 30, Yano teaches a first electrode terminal being separated from the isolation diffusion region. Regarding the claimed limitation of "the device is a diode", it is noted that independent claim 1 recites a power device. Clearly, a diode is not a power device. Therefore, it is understood that the diode is part of the power device. Thus, Yano's structure comprises a diode (e.g. layers 16 and 18 form a diode).

Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yano, Gross and Patterson, as applied to claims 1 and 26 above, and further in view of Collins (5,262,754).

Yano, Gross and Patterson teach substantially the entire claimed structure, as applied to claims 1 and 26 above, except a passivation layer includes a polymid layer over the oxide layer.

Collins teaches using a polymid layer when packaging the device (column 2, lines 50-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a polymid layer when packaging the device, such that the passivation layer includes a polymid layer over the oxide layer, in prior art's device in order to provide better protection for the device.

Claims 1-3, 25-26, 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) in view of Gross (5,316,964) and Patterson (4,972,247).

AAPA teaches in figure 1 and related text a power device, comprising:

a semiconductor substrate 1 of first conductivity having an upper surface and a lower surface;

a first electrode terminal 7 coupled to a first conductive region 5 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal 16 coupled to a second conductive region 15 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region 2 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

a passivation layer 17 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

AAPA does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, in AAPA's device in order to provide better protection to the device and to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 26, prior art's device includes a passivation layer includes an oxide layer and contacts the upper surface of the substrate, the first surface of the isolation diffusion region, and the peripheral junction region.

Regarding claim 28, the claimed limitations of "the peripheral junction region is provided to compensate the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region" are inherent in prior art's device, because prior art's device comprises a peripheral junction region which compensates the surface depletion of dopants in the isolation diffusion region and increase a reverse blocking voltage of the device by reducing an electric field at the first surface of the isolation diffusion region, as claimed.

Regarding claim 30, AAPA teaches a first electrode terminal being separated from the isolation diffusion region. Regarding the claimed limitation of "the device is a diode", it is noted that independent claim 1 recites a power device. Clearly, a diode is not a power device. Therefore, it is understood that the diode is part of the power device. Thus, AAPA's structure comprises a diode (e.g. layers 15 and 1 form a diode).

Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, Gross and Patterson, as applied to claims 1 and 26 above, and further in view of Collins (5,262,754).

AAPA, Gross and Patterson teach substantially the entire claimed structure, as applied to claims 1 and 26 above, except a passivation layer includes a polymid layer over the oxide layer.

Collins teaches using a polymid layer when packaging the device (column 2, lines 50-55).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a polymid layer when packaging the device, such that the passivation layer includes a polymid layer over the oxide layer, in prior art's device in order to provide better protection for the device.

Claims 1 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akiyama (5,994,189) in view of Gross and Patterson.

Regarding claim 1, Akiyama teaches in figure 1 and related text a power device, comprising:

a semiconductor substrate 2 of first conductivity having an upper surface and a lower surface;

a first electrode terminal 11 coupled to a first conductive region 4 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal 13 coupled to a second conductive region 1 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

an isolation diffusion region 7 of second conductivity P provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and

a passivation layer 10 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Akiyama does not teach a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions.

Gross teaches in figure 2 and related text a peripheral junction region of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, in Akiyama's device in order to provide better protection to the device and to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 30, Akiyama teaches in figure 1 and related text a device being a diode 1, 2, 4, wherein the first electrode terminal being separated from the isolation diffusion region.

Claims 1 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori et al. (5,101,244) in view of Gross and Patterson.

Regarding claim 1, Mori et al. teach in figure 1A and related text a power device, comprising:

a semiconductor substrate 14 of first conductivity having an upper surface and a lower surface;

a first electrode terminal 3 coupled to a first conductive region 16 provided proximate the upper surface of the substrate, the first electrode terminal being provided over the upper surface of the substrate;

a second electrode terminal 2 coupled to a second conductive region 13 provided proximate the lower surface of the substrate, the second electrode terminal being provided below the lower surface of the substrate;

a passivation layer 4 provided over the upper surface of the substrate, the first surface of the isolation diffusion region;

wherein the first and second electrode terminals define a vertical electrical current path there between, and

wherein the peripheral junction region is provided to compensate the surface depletion of the isolation diffusion region.

Mori et al. do not teach an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface; and a peripheral junction region of second conductivity formed at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, wherein the peripheral junction region is different than the first and second conductive regions.

Gross teaches in figure 2 and related text an isolation diffusion region 16, 17 of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity N+ formed at least partly within an N type isolation diffusion region 16, 17 and formed proximate the first surface of the isolation diffusion region.

Patterson teaches in figure 2 and related text an isolation diffusion region 12 of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity 19 formed at least partly within an isolation diffusion region 12 and formed proximate the first surface of the isolation diffusion region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an isolation diffusion region of second conductivity provided at a periphery of the substrate and extending from the upper surface to the lower surface of the substrate, the isolation diffusion region having a first surface corresponding to the upper surface of the substrate and a second surface corresponding to the lower surface, and a peripheral junction region of second conductivity at least partly within the isolation diffusion region and formed proximate the first surface of the isolation diffusion region, in Mori et al.'s device in order to provide

protection to the diode and in order to increase the electrical isolation capabilities of the device.

The combination is motivated by the teachings of Gross who points out the advantages of using a peripheral junction region within the isolation junction region (column 2, lines 38-41).

Note that prior art's device includes a peripheral junction region being different than the first and second conductive regions.

Regarding claim 30, Mori et al. teach in figure 1A and related text a device being a diode, wherein the combined device includes the first electrode terminal being separated from the isolation diffusion region (see Patterson et al.).

Response to Arguments

Some of applicant's arguments were adequately addressed in previous office actions, and the rest of applicant's arguments with respect to claims 1-3, 25-26, 28 and 30 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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/ORI NADAV/
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TECHNOLOGY CENTER 2800